REMARKS

Applicant respectfully requests reconsideration of this application, in view of the following remarks.

The drawings are objected to under 37 CFR § 1.84(p)(5) as not including references mentioned in the description. Figure 3c is objected to as duplicative of Figure 3b.

Claims 1-11 stand rejected under 35 USC § 102(e) as being anticipated by U.S. Patent 6,115,823 to Velasco et al. (Velasco).

In the Drawings

Figures 3c and 6 have been amended. Applicants request approval of the drawings and withdrawal of the objections. If the Examiner approves of the drawings, notification of such approval to the draftsperson, per enclosed letter is requested.

In the Claims

Claims 1-11 rejection under 35 U.S.C. § 102(e)

The Examiner has cited Velasco as teaching "a modular bus", "library modules to decrease design time", "a configurable interface that provides alternative single-edge and double-edge First-In-First-Out buffers", and that Velasco teaches that his "device is highly configurable regarding the claimed signal enabling, function enabling, and parametrization". (Office Action, page 3. See cited Velasco, col. 4, line 49 to col. 5, line 2; col. 22, line 60 and following; col. 32, line 48 and following; and col. 35, lines 47-60.)

Applicants believe that Velasco may be misunderstood with respect to the Applicants invention.

There is a distinction between "configurability of the interface" (the present invention) and "configurability of the core" (Velasco).

Claim 1:

Applicants' claim 1 recites:

> 1. A computer core comprising at least one interface signal that is configurable such that the interface signal can be selectively present.
> (Emphasis added.)

First, Velasco does not disclose an interface signal or a group of signals that are selectively present at the interface. Velasco at Table III (col. 37-39) clearly indicates in column 3 of the table that all interface signals are required. All signals required is different than a signal that can be selectively present.

Second, in comparing Velasco Fig. 36 and 37, which represent two extremes of the type of "configurality" that Velasco describes (single-edge v. dual-edge data transfer), the signals at the interface are the same. Thus, Velasco does not describe an interface signal that is configurable and can be selectively present.

For these reasons, Applicants submit that claim 1 and its dependents are allowable over the cited art.

Claim 4:

Applicants' claim 4 recites:

4. A computer core comprising at least one interface signal that is configurable such that the interface signal can be configured to support different levels of functionality.
(Emphasis added.)

First, Applicants find no reference in Velasco for interface signal configurability to support different levels of functionality. Velasco describes a configurable core that uses the same interface signals and encodings in different ways, but where the interface remains the same (as noted in Table III col. 37-39). In the description of the function of the interface signals in Velasco, there is no mention of any particular interface signal being used in different ways depending on configuration options specified by the user.

Second, while Velasco refers to a "Parameterized synchronous or asynchronous FIFO" (col. 35, lines 49-50), this is an internal configurability option that has no impact on the interfaces.

Third, while Valesco refers to a "Parameterized RAM size and RAM data bus width" (col. 35, lines 50-51), this is a configurability option that changes the internals of the core, not the interface.

Fourth, while Velasco refers to a "Parameterized data rate transfer (either singular (positive) edge clocking or dual-edge clocking)" (col. 35, lines 51-52), this is an internal configurability option that decides how the particular clock signals are used, but it has no impact on the interface signals in a function-enabling or signal-enabling way.

Further, while Velasco refers (col. 35, lines 52-60) to "configurable to support different combinational Write Parameter RAM and Write Data RAM, or Write

Parameter RAM and Read Data RAM, or write data RAM only without read", "Flushing of current FIFO request, and flushing of entire FIFO requests may be used in case error occurs", and "Parameterized control bit register "enough space acknowledge" (req_esp_ack) to indicate FIFO go-ahead to request target access even if not all write data is in the memory yet", these are all internal configurability options that have no impact on the interface-signals.

For all these reasons, Applicants submit that claims 4 and 5 are distinguished over the cite art and are allowable.

Claim 6:

Applicants' claim 6 recites:

> 6. A computer core comprising at least one interface signal, a signal width of the at least one interface signal being configurable to support different signal widths.
> (Emphasis added.)

As noted above, Velasco discloses a "Parameterized RAM size and RAM data bus width", however this is a configurability option that changes the internals of the core not the interface signal. Thus, Applicants submit that claim 6 is allowable over the cited art.

Claims 7-11:

Claims 7 through 11 are method claims for generating the configurable interface. Thus, for all the reasons enumerated above, Velasco does not disclose

this configurable interface nor the method for generating the configurable interface. Therefore Applicants submit that claims 7-11 are allowable over the cited art.

CONCLUSION

For the foregoing reasons, Applicants respectfully submit that all claims are in condition for allowance. Allowance of all claims is respectfully requested.

If there are any additional charges/credits, please charge/credit our deposit account no. 02-2666. If any extensions of time are necessary, authority is given to take such.

Respectfully submitted,
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification

Please replace the last paragraph starting on page 9 and extending to the top of page 10 with the following:

One embodiment of a method of generating the optimal core is illustrated in **Figure 6**. At step 610, the core source code with at least one configurable interface parameter is provided. In one embodiment, for each interface configuration option, a parameter is defined, together with a range of allowable values. For example, for configuring the width the MData field of **Figure 4**, the parameter name MData_WIDTH is defined and the allowable values are 8,16,32 and 64. For signal-enabling the MBurst field, the parameter MBurst_ENABLE can be defined with the allowable values of 0 and 1, where the value 0 indicates that it is not present and the value of 1 indicates that it is.